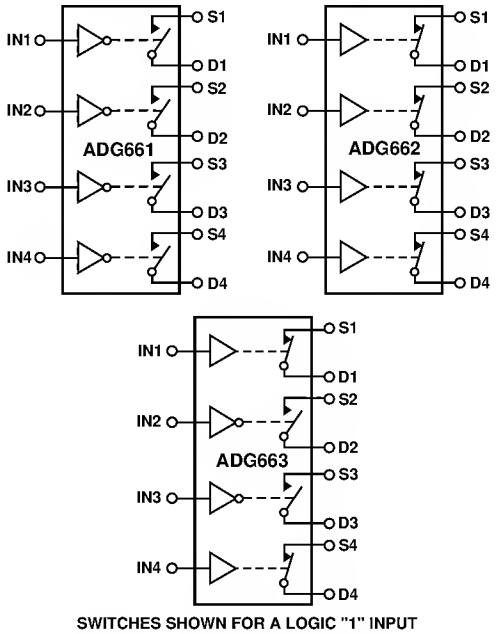
LC²MOS
Precision 5 V Quad SPST Switches

ADG661/ADG662/ADG663

FEATURES
+5 V, ±5 V Power Supplies
Ultralow Power Dissipation (<0.5 μW)
Low Leakage (<100 pA)
Low On Resistance (<50 Ω)
Fast Switching Times
Low Charge Injection
TTL/CMOS Compatible
TSSOP Package

APPLICATIONS
Battery Powered Instruments
Single Supply Systems
Remote Powered Equipment
+5 V Supply Systems
Computer Peripherals such as Disk Drives
Precision Instrumentation
Audio and Video Switching
Automatic Test Equipment
Precision Data Acquisition
Sample Hold Systems
Communication Systems

FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG661, ADG662 and ADG663 are monolithic CMOS devices comprising four independently selectable switches. These switches feature low, well-controlled on resistance and wide analog signal range, making them ideal for precision analog signal switching.

They are fabricated using Analog Devices' advanced linear compatible CMOS (LC²MOS) process, which offers benefits of low leakage currents, ultralow power dissipation and low capacitance for fast switching speeds with minimum charge injection.

The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. Fast switching speed coupled with high signal bandwidth also make the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

The ADG661, ADG662 and ADG663 contain four independent SPST switches. The ADG661 and ADG662 differ only in that the digital control logic is inverted. The ADG661 switches are turned on with a logic low on the appropriate control input, while a logic high is required for the ADG662. The ADG663 has two switches with digital control logic similar to that of the ADG661, while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when ON and has an input signal range that extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. +5 V Single Supply Operation
   The ADG661, ADG662 and ADG663 offer high performance, including low on resistance and wide signal range, fully specified and guaranteed with ±5 V and +5 V supply rails.
2. Ultralow Power Dissipation
   CMOS construction ensures ultralow power dissipation.
3. Low R_{ON}
4. Break-Before-Make Switching
   This prevents channel shorting when the switches are configured as a multiplexer.

REV. 0

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ADG661/ADG662/ADG663– SPECIFICATIONS[1]

Dual Supply (V_{DD} = +5 V ± 10%, V_{SS} = – 5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Versions +25°C	B Versions –40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{DD} to V_{SS}	V	
R_{ON}	30		Ω typ	V_D = –3.5 V to +3.5 V, I_S = –10 mA;
	38	50	Ω max	V_{DD} = +4.5 V, V_{SS} = –4.5 V
LEAKAGE CURRENTS				V_{DD} = +5.5 V, V_{SS} = –5.5 V
Source OFF Leakage I_S (OFF)	±0.025		nA typ	V_D = ±4.5 V, V_S = ±4.5 V;
	±0.1	±2.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.025		nA typ	V_D = ±4.5 V, V_S = ±4.5 V;
	±0.1	±2.5	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.05		nA typ	V_D = V_S = ±4.5 V;
	±0.2	±5	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	150		ns typ	R_L = 300 Ω, C_L = 35 pF;
		275	ns max	V_S = ±3 V; Test Circuit 4
t_{OFF}	55		ns typ	R_L = 300 Ω, C_L = 35 pF;
		120	ns max	V_S = ±3 V; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG663 Only)	80		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +3 V; Test Circuit 5
Charge Injection	6		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	70		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	90		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		pF typ	f = 1 MHz
C_D (OFF)	9		pF typ	f = 1 MHz
C_D, C_S (ON)	28		pF typ	f = 1 MHz
POWER REQUIREMENTS				
		+4.5/5.5	V min/max	
V_{DD}		–4.5/5.5	V min/max	
I_{DD}	0.0001		µA typ	V_{DD} = +5.5 V, V_{SS} = –5.5 V
		1	µA max	Digital Inputs = 0 V or 5 V
I_{SS}	0.0001		µA typ	
		1	µA max	

NOTES

[1]Temperature ranges are as follows: B Versions, –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Single Supply (V_{DD} = +5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted)

Parameter	B Versions +25°C	B Versions –40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
R_{ON}	45		Ω typ	V_D = 0 V to +3.5 V, I_S = –10 mA;
	68	75	Ω max	V_{DD} = +4.5 V
LEAKAGE CURRENTS				V_{DD} = +5.5 V
Source OFF Leakage I_S (OFF)	±0.025		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
	±0.1	±2.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.025		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
	±0.1	±2.5	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.05		nA typ	V_D = V_S = +4.5 V/+1 V;
	±0.2	±5	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	250		ns typ	R_L = 300 Ω, C_L = 35 pF;
		400	ns max	V_S = +2 V; Test Circuit 4
t_{OFF}	45		ns typ	R_L = 300 Ω, C_L = 35 pF;
		100	ns max	V_S = +2 V; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG663 Only)	140		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +2 V; Test Circuit 5
Charge Injection	12		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	70		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	90		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		pF typ	f = 1 MHz
C_D (OFF)	9		pF typ	f = 1 MHz
C_D, C_S (ON)	28		pF typ	f = 1 MHz
POWER REQUIREMENTS				
V_{DD}		+4.5/5.5	V min/max	
I_{DD}	0.0001		µA typ	V_{DD} = +5.5 V
		1	µA max	Digital Inputs = 0 V or 5 V

NOTES
[1]Temperature ranges are as follows: B Versions, –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} ..... +44 V
V_{DD} to GND ..... –0.3 V to +25 V
V_{SS} to GND ..... +0.3 V to –25 V
Analog, Digital Inputs[2] ..... V_{SS} –2 V to V_{DD} +2 V or 30 mA, Whichever Occurs First
Continuous Current, S or D ..... 30 mA
Peak Current, S or D ..... 100 mA
(Pulsed at 1 ms, 10% Duty Cycle max)
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
TSSOP Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 115°C/W
θ_{JC} Thermal Impedance ..... 35°C/W
Lead Temperature, Soldering
Vapor Phase (60 secs) ..... +215°C
Infrared (15 secs) ..... +220°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG661BRU	–40°C to +85°C	16-Lead TSSOP	RU-16
ADG662BRU	–40°C to +85°C	16-Lead TSSOP	RU-16
ADG663BRU	–40°C to +85°C	16-Lead TSSOP	RU-16

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG661/ADG662/ADG663 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

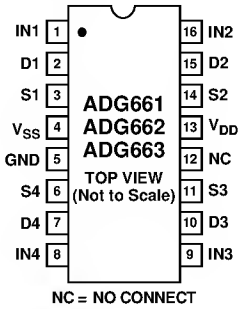


Table I. Truth Table (ADG661/ADG662)

ADG661 In	ADG662 In	Switch Condition
0	1	ON
1	0	OFF

Table II. Truth Table (ADG663)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
R_{ON}	Ohmic resistance between D and S.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	"OFF" Switch Source Capacitance.
C_D (OFF)	"OFF" Switch Drain Capacitance.
C_D, C_S (ON)	"ON" Switch Capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on.
t_{OFF}	Delay between applying the digital control input and the output switching off.
t_D	"OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to analog output during switching.

Typical Performance Characteristics

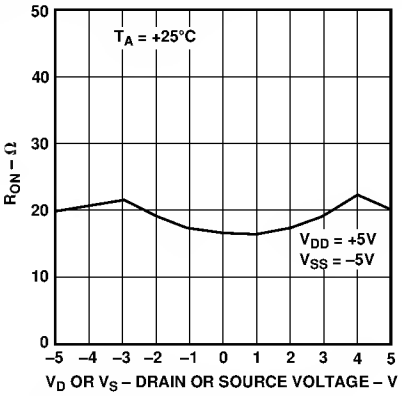


Figure 1. On Resistance as a Function of V_D (V_S) Dual Supplies

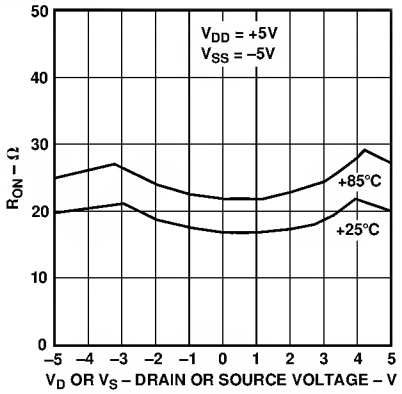


Figure 2. On Resistance as a Function of V_D (V_S) for Different Temperatures

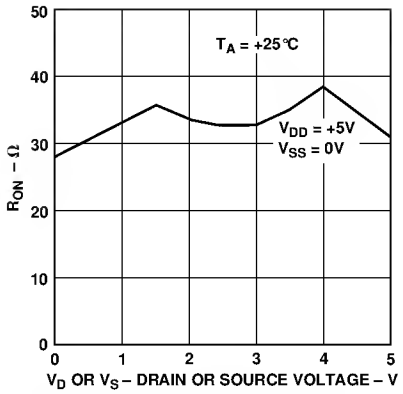


Figure 3. On Resistance as a Function of V_D (V_S) Single Supply

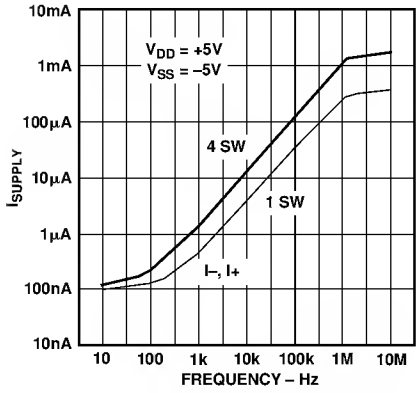


Figure 4. Supply Current vs. Input Switching Frequency

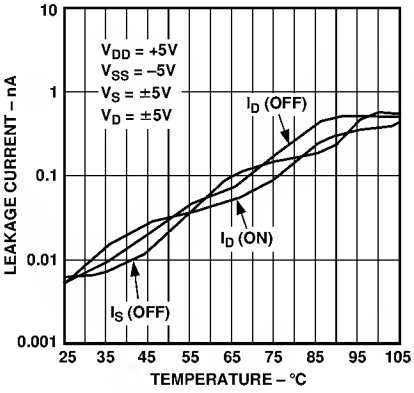


Figure 5. Leakage Currents as a Function of Temperature

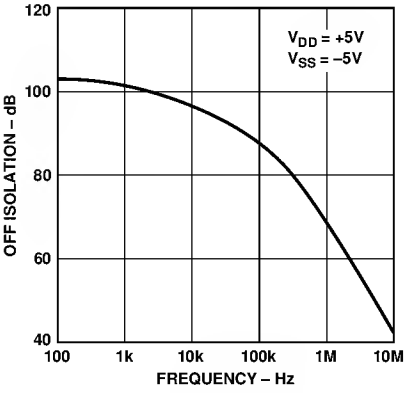


Figure 6. Off Isolation vs. Frequency

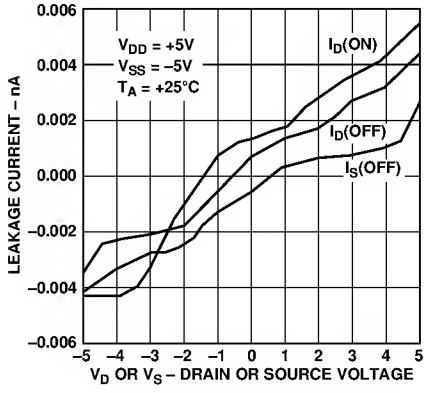


Figure 7. Leakage Currents as a Function of V_D (V_S)

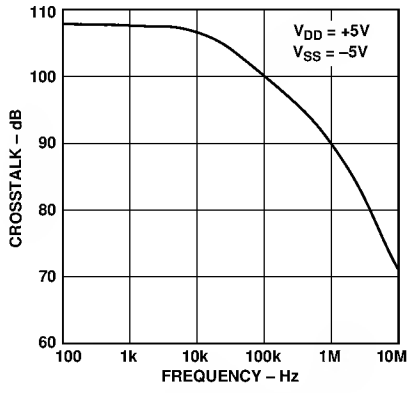
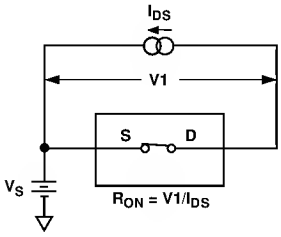
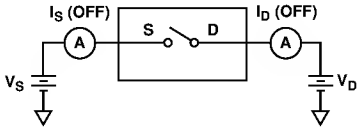


Figure 8. Crosstalk vs. Frequency

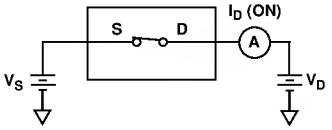
Test Circuits



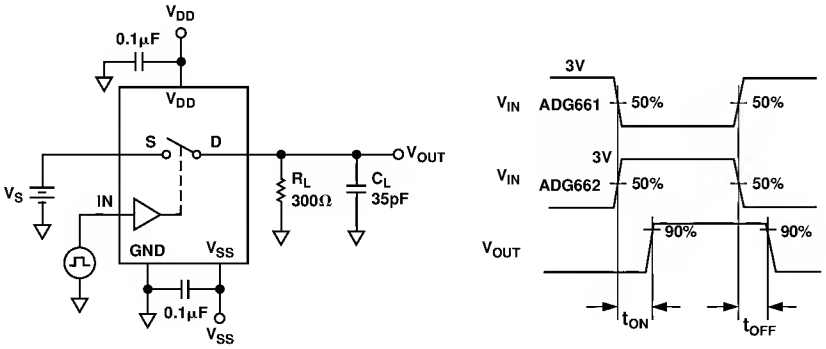
1. On Resistance



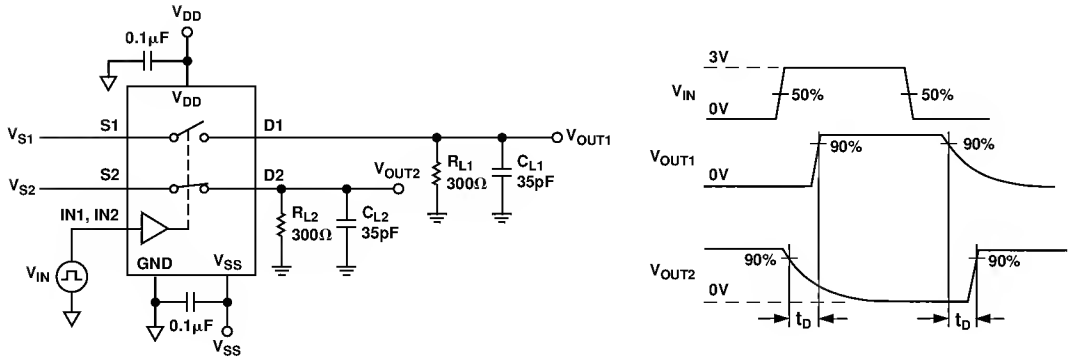
2. Off Leakage



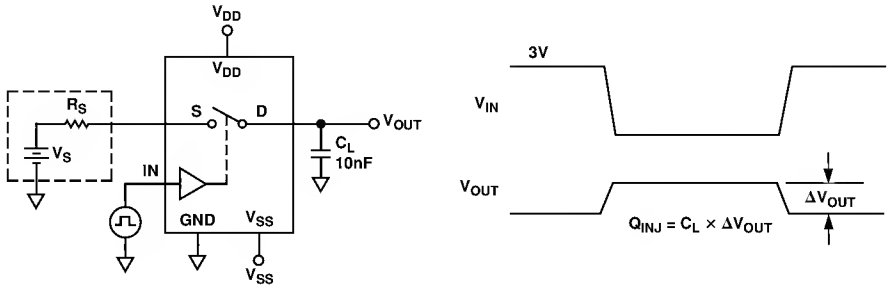
3. On Leakage



4. Switching Times

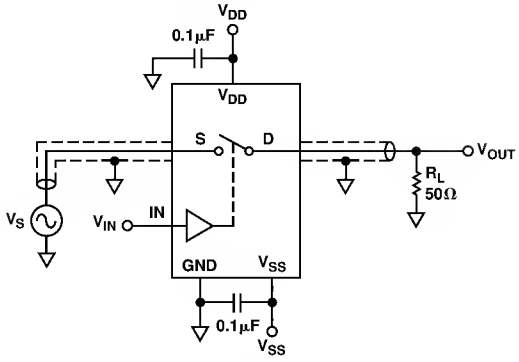


5. Break-Before-Make Time Delay

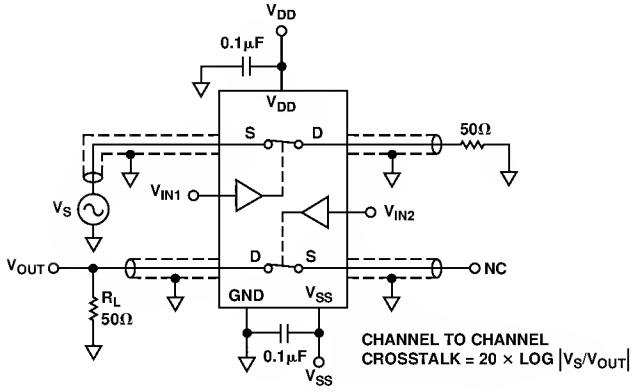


6. Charge Injection

Test Circuits (Continued)



7. Off Isolation



8. Channel-to-Channel Crosstalk

APPLICATION

Figure 9 illustrates a precise, sample-and-hold circuit. An AD845 is used as the input buffer while the output operational amplifier is an OP07. During the track mode, SW1 is closed and the output V_{OUT} follows the input signal V_{IN}. In the hold mode, SW1 is opened and the signal is held by the hold capacitor C_H.

Due to switch and capacitor leakage, the voltage on the hold capacitor will decrease with time. The ADG661/ADG662/ADG663 minimizes this droop due to its low leakage specifications. The droop rate is further minimized by the use of a polystyrene hold capacitor. The droop rate for the circuit shown is typically 15 μV/μs.

A second switch SW2, which operates in parallel with SW1, is included in this circuit to reduce pedestal error. Since both switches will be at the same potential, they will have a differential effect on the op amp OP07 which will minimize charge injection effects. Pedestal error is also reduced by the compensation network R_C and C_C. This compensation network also reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the ±3 V input range. The acquisition time is 2.5 ms while the settling time is 1.85 μs.

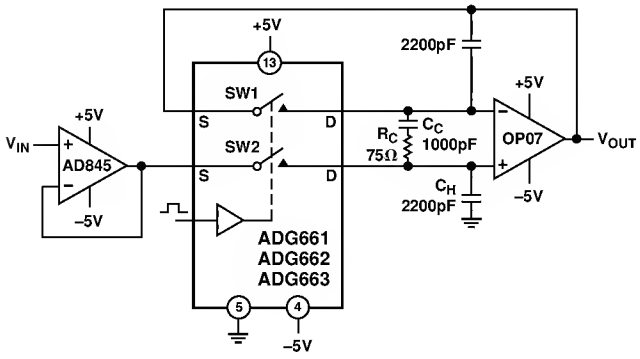
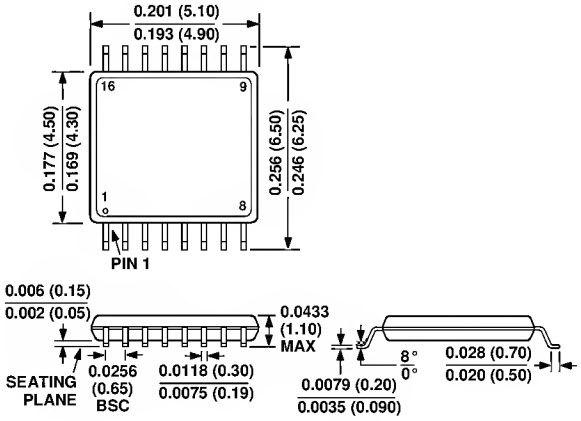


Figure 9. Accurate Sample-and-Hold

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead TSSOP
(RU-16)



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